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(54) Semiconductor memory device including main/sub-bit line arrangement

(57) A semiconductor memory device comprises a plurality of sub-bit lines, a sense amplifier provided in common to the plurality of sub-bit lines and receiving a data signal from a first one of the plurality of sub-bit lines, a main-bit lines operatively coupled to the sense amplifier to receive an output of the sense amplifier, and a data latch circuit provided to latch data appearing on the main-bit line. The device further comprises means for transferring a data signal of a second one of the plurality of sub-bit lines to the sense amplifier during the data latch circuit being accessed to read out data latched in the data latch circuit.

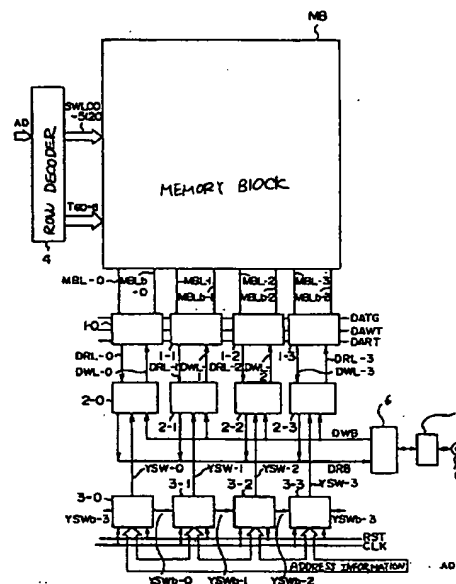


Fig. 4

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## Description

### BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor memory device and, more specifically, to a dynamic random-access memory (DRAM) having memory cells each constructed of 1 (one) transistor and 1 (one) capacitor.

DRAMs have been increased in integration density year by year, so that DRAMs of 1G bits have been developed. In order to increase memory capacities, each of cell areas is required to be reduced and line pitches of word lines and of bit lines are also required to be small. As is well known in the field of DRAMs, data stored in an accessed memory cell should be sensed so as to be read, this data should be rewritten into the memory cell. Furthermore, data stored in another memory cells connected to the same word line must be sensed and be rewritten in the the another memory cells. The above-explained operation is carried out by sense amplifiers. Since the sense amplifiers are constituted by a plurality of transistors, regions shared by these sense amplifiers would impede reductions of pitches of bit lines.

Accordingly, such an idea is conceivable that a plurality of bit lines are commonly used by a single sense amplifier. However, in this case, the data should be rewritten into a plurality of memory cells connected to the selected word line in the time divisional manner. Accordingly, this idea is not adapted to such a memory that access addresses are changed in non-continuous manner. To the contrary, for instance, this idea may be realized as a file memory. In a file memory, when access addresses are changed in the continuous manner, the change in the address can respond to the above-described time divisional control of data sensing/data writing operations. Thus, it is possible to provide file memories with large storage capacities.

Fig. 1 schematically shows the above-described one conventional DRAM. It should be noted in this DRAM that bit lines are constructed of main-bit/sub-bit line arrangement, and a single sense amplifier is commonly used by a plurality of sub-bit lines. This DRAM owns a memory block MB and a peripheral circuit thereof. This memory block MB will be discussed later in detail with reference to Fig. 2. A plurality of main-bit line pair MBL-i, MBLb-i (i=0, 1,...) are derived from this memory block MB. These main-bit line pair MBL and MBLb are connected to a switch circuit corresponding to switch circuits 10-i. These switch circuits 10-i are commonly connected via data bus pair DB, DBb to a data read/write amplifier 14. The data read/write amplifier 14 is connected via an input/output buffer 15 to an input/output pin 16, so that data is transmitted between the data read/write amplifier 14 and the input/output pin 16. One switch circuit of the switch circuits 10-i is selected by an address in response to a switch selecting signal YSW-i sent from a column decoder 12. A word

line selecting signal SWL and memory switching signals TG<sub>0</sub> to TG<sub>3</sub> are supplied from a row decoder 13 to the memory block MB.

The operations of this peripheral circuit are the same as those of the usual DRAM. That is, the row decoder 13 drives one word line selecting signal SWL<sub>00</sub> based on the address information. In response to this driving operation, data of the selected memory cell are read to the respective main bit line pair MBL, MBLb. On the other hand, the column decoder 12 selects the main bit line pair MBL, MBLb via one switch circuit 10 to be connected with the data bus pair DB, DBb. The input/output buffer 15 output the read data to the input/output pin 16 based upon the data appearing on the selected main bit line pair MBL, MBLb in the data read mode, whereas the data amplifier 14 drive the main bit line pair based on the write data to the input/output pin 16 in the data write mode.

In Fig. 2, there is shown an arrangement related to the main bit line pair MBL-0, MBLb-0 as a portion of the memory block MB. This memory block is a so-called "open bit system". Four sub-bit lines SBL<sub>0</sub> to SBL<sub>3</sub> are extended on both sides of a single sub-sense amplifier 17a, while commonly using this sub-sense amplifier 17a. The word line SWL is intersected with these bit lines SBL<sub>0</sub> to SBL<sub>3</sub>, and then a DRAM memory cell MC constructed of one transistor and one capacitor is provided with each of cross points. Since one sense amplifier 17a is commonly used, the sub-bit lines SBL<sub>0</sub> to SBL<sub>3</sub> are connected via pMOS transistors T<sub>TG0</sub> to T<sub>TG3</sub> to the sub-sense amplifier 17a, and these transistors T<sub>TG0</sub> to T<sub>TG3</sub> are turned ON/OFF in response to the memory switching signals TG<sub>0</sub> to TG<sub>3</sub>. The subsense amplifier 17a includes a precharge circuit P<sub>2</sub> for precharging this one pair of input/output modes, and NMOS transistors T<sub>n20</sub> and T<sub>n21</sub> for amplifying the level of the selected sub-bit line. This sub-sense amplifier 17a further contains nMOS transistors T<sub>n22</sub> to T<sub>n25</sub> for controlling connection/disconnection between the selected sub-bit line and main bit line pair MBL-0, MBLb-0. The nMOS transistors T<sub>n22</sub> and T<sub>n23</sub> are conducted by the signal RS when the amplified level of the sub-bit line is transferred to the main bit line, whereas the nMOS transistors T<sub>n24</sub> and T<sub>n25</sub> are conducted by the signal WS when the data is rewritten. A main sense amplifier 18a is connected to the main bit line pair MBL-0 and MBLb-0. This main sense amplifier 18a includes a main bit line precharge circuit P<sub>1</sub>, pMOS transistors T<sub>p20</sub>, T<sub>p21</sub> and nMOS transistors T<sub>n26</sub>, T<sub>n27</sub>, which are provided between sense amplifier drive lines SAP and SAN, and are connected to form a flip-flop. Each of the precharge circuits P<sub>1</sub> and P<sub>2</sub> precharges the input/output mode of the corresponding sense amplifier to a V<sub>cc</sub>/2-level.

Referring now to a timing chart of Fig. 3, data reading operation of this DRAM will be described.

In a reset period before the data reading operation, all of the word lines SWL and the memory switching signals TG are at low levels, and the input/output modes of

the respective sense amplifiers are precharged to  $V_{cc}/2$ .

Next, the precharge circuit  $P_1$ ,  $P_2$  becomes inactive, and one word line, for instance,  $SWL_{00}$  is selected to become a high level. Furthermore, the switching signal  $TG_0$  becomes a low level. As a result, a memory cell  $MC_{000}$  located at a cross point between this word line  $SWL_{00}$  and the sub-bit line  $SBL_0$  is selected, and thus, the potential of the sub-bit line  $SBL_0$  becomes such a potential corresponding to the data stored in this selected memory cell  $MC_{000}$ . On the other hand, the sub-bit line  $SBL_0$  located on the lower side of the sub-sense amplifier 17a holds the precharge level. Accordingly, a potential difference is produced at the input/output mode of the sub-sense amplifier 17a. Under this condition, the read signal  $RS$  becomes active, so that the transistors  $T_{n22}$  and  $T_{n23}$  are conducted. As a consequence, this potential difference is transferred to the main-bit line pair  $MBL$  and  $MBLb$ . The sense amplifier drive lines  $SAP$  and  $SAN$  becomes active levels, and the levels of the main bit line pair  $MBL$  and  $MBLb$  are amplified by the main sense amplifier 18a.

Thereafter, the read signal  $RS$  becomes a low level and the write signal  $WS$  becomes a high level, and the respective levels of the main-bit line pair  $MBL$ ,  $MBLb$  are transferred via the transistors  $T_{n24}$  and  $T_{n25}$  to the sub-bit line  $SBL_0$ , so that the data is rewritten into the memory cell  $MC_{000}$ .

It should be understood that in this memory block  $MB$  all of the upper circuit portions from the main sense amplifier 18a are made by the nMOS structure so as to further reduce the chip area. As a result, the sub-sense amplifier 17a owns no function to rewrite data. However, if a slight increase in the chip area is allowable, then the sub-sense amplifier 17a may be substituted by the main-sense amplifier 18a.

On the other hand, in the peripheral circuit, the addresses to the column decoder 12 are sequentially changed during a time period ( $T_1$ ) when the write signal  $WS$  is at the high level to thereby sequentially select the switch circuit 10, so that the data appearing on the main bit line pair  $MBL$ ,  $MBLb$  are successively outputted. When the data transfer is ended, the writer signal  $WS$  is set to a low level, so that the respective main bit line pair  $MBL$ ,  $MBLb$  are precharged to  $V_{cc}/2$ . Thereafter, as described above, the memory switching signal  $TG_1$  becomes a high level, so that the data are read out in the continuous manner.

However, in the above-described memory, the respective main bit line pair  $MBL$ ,  $MBLb$  must be precharged so as to be initialized every time the signals for causing the switching signals  $TG_0$  to  $TG_4$  to become the active levels are switched. Accordingly, the data cannot be continuously read from all of the cells connected to the selected word line, so that the rest time period is required in the data reading operation, as indicated by " $t_4$ " of Fig. 3.

## SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide a semiconductor memory device, the reading efficiency of which is further increased, as compared with that of the conventional semiconductor memory device.

A semiconductor memory device of the present invention comprises a plurality of sub-bit lines; a sense amplifier provided in common to the plurality of sub-bit lines and receiving a data signal from a first one of the plurality of sub-bit lines; a main-bit line operatively coupled to the sense amplifier to receive an output of the sense amplifier; a data latch circuit provided to latch data appearing on the main-bit line; and means for transferring a data signal of a second one of the plurality of sub-bit lines to the sense amplifier during the data latch circuit being accessed to read out data latched in the data latch circuit.

Another semiconductor memory device of the present invention comprises a plurality of sub-bit lines; a sense amplifier provided in common to the plurality of sub-bit lines; a main-bit line coupled to said sense amplifier; a data latch circuit temporarily latching first data to be written, first means for transferring the first data from the data latch circuit to the main bit line to thereby allow the sense amplifier to drive a first one of the sub-bit lines in response to the first data; and second means for disconnecting the data latch circuit from the main-bit line during the data latch circuit being controlled to latch second data to be written, to thereby allow the sense amplifier prepare driving a second one of the sub-bit lines in response to the second data.

As described above, once the data of the main bit line is latched by the latch circuit, the main bit become free no longer the read data of the main-bit line must be held. Accordingly, after the read data has been latched by the latch circuit, the main bit line can be initialized, so that the next sub-bit line can be accessed immediately. As a result, the initialization time period ( $t_1$ ) of the main-bit line does not need.

## BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages, and features of the present invention will be more apparent from the following descriptions to be read in conjunction with the accompanying drawings, in which:

Fig. 1 is the schematic block diagram for showing the conventional DRAM;

Fig. 2 is the circuit diagram of the memory block  $MB$  shown in the DRAM of Fig. 1;

Fig. 3 is the timing chart for representing the reading operation of the DRAM indicated in Fig. 1;

Fig. 4 is a schematic block diagram for showing a DRAM according to a first embodiment of the present invention;

Fig. 5 is a circuit diagram of the latch circuit

employed in the DRAM of Fig. 4;

Fig. 6 is a circuit diagram of the switch circuit employed in the DRAM of Fig. 4;

Fig. 7 is a circuit diagram of the switch selection circuit employed in the DRAM of Fig. 4;

Fig. 8 is a timing chart for indicating data reading operation of the DRAM shown in Fig. 4;

Fig. 9 is a timing chart for indicating data writing operations of the DRAM shown in Fig. 4;

Fig. 10 is a circuit diagram for producing the data latch signal indicated in Fig. 4;

Fig. 11 is a timing chart for indicating the data latch signal generation timing of the data latch signal generating circuit employed in the DRAM of Fig. 4;

Fig. 12 is a circuit diagram for showing another data latch signal generating circuit;

Fig. 13 is a data read timing chart for the DRAM by way of the data latch signal generating circuit of Fig. 12; and

Fig. 14 is a data write timing chart for the DRAM by way of the data latch signal generating circuit of Fig. 12.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 4 schematically represents a block diagram of a DRAM according to a first embodiment of the present invention. It should be noted that the same reference numerals shown in Fig. 1 will be employed as those for denoting the same or similar constructive units, and explanations thereof are omitted. In this embodiment, the respective main-bit line pair MBL, MBLb derived from a memory block MB are connected to data latch circuits 1, respectively. A data write signal DAWT, a data read signal DART, and a data latch signal DATG are commonly supplied to each of the data latch circuit 1. When the signal DATG is in an active level, the main bit line pair MBL, MBLb are electrically connected to the data latch circuits 1. At this time, when a data read signal DART becomes an active level, data appearing on the main-bit line pair MBL, MBLb are latched in the data latch circuits 1 and transferred to a data read line DRL. On the other hand, when the data write signal DAWT is in active level, the write data of the data write line DWL is latched in the data latch circuits 1 and transferred to the main-bit line pair MBL, MBLb. The data read line DRL and the data write line DWL are connected to switch circuits 2, respectively. These switch circuits 2 are controlled in response to switch selecting signals YSW and to connect lines DRL and DWL to a data read bus DRB and a data write bus DWB, respectively when the signals YSW is active level. The respective switch selecting signals YSW are produced by switch selecting circuits 3. The switch selecting circuits produce a transfer signal complementary to the switch selecting signal YSW. The transfer signal YSWb of the prestages circuit 3 are inputted to the post-staged circuit 3. Furthermore, an address information AD, a clock sig-

nal CLK, and a reset signal RST are commonly supplied to the switch selecting circuits 3. The data read bus DRB and the data write bus DWB are connected to a data read/write amplifier 6, so that the read data/write data are supplied via an input/output buffer 7 between this data read/write amplifier 6 and an input/output pin 8.

Since the switch selecting circuits 3 are arranged as described above, all of these switch selecting circuits 3 can be reset by a reset signal RST so that the switch selecting circuits 3 is set the signal YSW non-active. In response to the address information AD, the switch selecting circuit 3 indicated the address information enforce the signal YSW High level. Therefore the switch selecting circuit 3 sets the transfer signal YSWb to low level. The post staged circuit 3 inputs the transfer signal YSW at the low level and outputs the signal YSW at high level. That is, the switch selecting circuit 3 may function as a shift register. For instance, the switch selecting circuit 3-0 selected to the address information sets the signal YSW<sub>0</sub> to a high level, so that the switch circuit 2-0 is selected. In response to the clock signal CLK, the next switch selecting circuit 3-1 is operated. Subsequently, the switch selecting circuits are successively brought into the active conditions, so that the corresponding switch circuits are successively turned ON.

It should also be noted that since an internal arrangement of the memory block MB is the same as that of Fig. 2, this internal arrangement is omitted.

Referring now to Fig. 5, each data latch circuit 1 includes nMOS transistors MN<sub>1</sub> and MN<sub>2</sub> with respect to the main-bit line pair MBL and MBLb. Either the data latch signal DATG is supplied to gates of these nMOS transistors MN<sub>1</sub> and MN<sub>2</sub>. Inverters IV<sub>1</sub> and IV<sub>2</sub> are connected to the transistors MN<sub>1</sub> and MN<sub>2</sub>. An nMOS transistor MN<sub>6</sub> is connected with the output of the inverter IV<sub>1</sub> and another nMOS transistor MN<sub>7</sub> is connected with the output of the inverter IV<sub>2</sub>. When the data read signal DART becomes active, these nMOS transistors MN<sub>6</sub> and MN<sub>7</sub> are activated, so that a flip-flop R<sub>1</sub> is formed by the inverter IV<sub>1</sub> and IV<sub>2</sub>. The output of the inverter IV<sub>1</sub> is connected via an inverter IV<sub>3</sub> to the data read line DRL. The output of the inverter IV<sub>2</sub> is connected to a dummy inverter IV<sub>4</sub>. It is provided which may make the load capacitances of the outputs of the inverters IV<sub>1</sub> and IV<sub>2</sub> equal to each other. On the other hand, an inverter IV<sub>5</sub> is provided with the data write line DWL. The output of this inverter IV<sub>5</sub> is connected to the inverter IV<sub>6</sub> and the nMOS transistor MN<sub>3</sub>. The output of the inverter IV<sub>6</sub> is connected to the nMOS transistor MN<sub>4</sub>. Moreover, the inverter IV<sub>6</sub> is connected via a MOS transistor MN<sub>5</sub> to the line DWL. That is, another flip-flop R<sub>2</sub> is formed by the inverters IV<sub>5</sub> and IV<sub>6</sub>. When the data write signal DAWT becomes active, the output of the inverter IV<sub>5</sub> is connected to the main bit line MBLb, and the output of the inverter IV<sub>6</sub> is connected to the main bit line MBL. The nMOS transistor MN<sub>5</sub> may function as a small resistor in order not transfer the high impedance condition of the data write line DWL to the flip-flop R<sub>2</sub> when

the write mode is not selected.

During the data reading operation, the signal DART becomes an active high level. Under this condition, a data latch signal DATG is produced as a one-shot pulse, so that the read data on the main-bit line pair MBL, MBLb is latched in the flip-flop  $R_1$ . In other words, since the data read signal DART is in a high level, (signal DAWT is in a low level), the transistors  $MN_6$  and  $MN_7$  are under ON state, so that the data of the selected memory cell is written into the flip-flop  $R_1$ . When the signal DATG is returned to the low level, the transistors  $MN_1$  and  $MN_2$  are turned OFF, so that the main bit line pair is disconnected from the latch circuit 1. The output from the flip-flop  $R_1$ , namely the output from the inverter  $IV_1$  is transferred via the inverter  $IV_2$  to the data read line DRL.

On the other hand, during the data writing operation, the data read signal DART becomes a low level and the data write signal DAWT becomes a high level, so that the write data is latched from the data write line DWL to the flip-flop  $R_2$ . This data written into the flip-flop  $R_2$  is transferred to the main-bit line pair MSL, MSLb when the data latch signal DATG becomes the high level.

Referring now to Fig. 6, the switch circuit 2 includes pMOS transistors  $M_{p1}$ ,  $M_{p2}$ , nMOS transistors  $M_{n8}$ ,  $M_{n9}$  and inverter  $IV_7$ . The transistors  $M_{p1}$ ,  $M_{n8}$  are provided between the data read line DRL and the data read bus DRB, and another pair of transistors  $M_{p2}$  and  $M_{n9}$  are provided between the data write line DWL and the data write bus DWB. The switch selecting signal YSW is coupled to the gates of the nMOS transistors  $M_{n8}$ ,  $M_{n9}$ , whereas a reverse signal of the switch selecting signal YSW is coupled to the gates of the pMOS transistors  $M_{p1}$ ,  $M_{p2}$ . Accordingly, when the switch selecting signal YSW is in a low level, all of these transistors become non-active, so that the signal path between the data read line DRL and the data read bus DRB, and the signal path between the data write line DWL and the data write bus DWB become non-active, respectively. Conversely, when the switch selecting signal YSW is in a high level, all of these transistors become active, so that the signal path between the data read line DRL and the data read bus DRB, and the signal path between the data write line DWL and the data write bus DRB are conducted, and thus the data are transferred through the respective signal paths.

Referring now to Fig. 7, the switch selecting circuit 3 is arranged by a data flip-flop DFF and an address decoder AD. The address decoder AD receives the address information, and when this address decoder AD is selected, the address decoder AD outputs a low level. The address decoder AD outputs a high level in any cases other than the above-described case. On the other hand, the transfer signal YSWb-1 is inputted via a gate  $G_3$  arranged by pMOS transistors  $M_{p3}$  and  $M_{n10}$  to a NAND circuit  $NAND_1$ . The NAND circuit  $NAND_1$  inputs the output from the address decoder AD and the transfer signal YSWb-1, and is connected to a node "S".

This node "S" is connected via an inverter  $IV_9$ , to the gate  $G_4$  arranged by a pMOS transistor  $M_{p6}$  and an nMOS transistor  $M_{n11}$ . This node S is further connected to a gate  $G_5$  arranged by a pMOS transistor  $M_{p4}$  and an nMOS transistor  $M_{n12}$ . The output of the inverter  $IV_{11}$  is connected to another inverter  $IV_{12}$ . The inverters  $IV_{11}$  and  $IV_{12}$  output the transfer signal YSWb and the switch selecting signal YSW, respectively. The output of the inverter  $IV_{11}$  is further connected to a NOR circuit  $NOR_1$ . The NOR circuit  $NOR_1$  inputs a reset signal RST and the transfer signal YSWb. The output of this NOR circuit  $NOR_1$  is connected the gate  $G_6$  arranged by an nMOS transistor  $M_{n13}$  and a pMOS transistor  $M_{p5}$ . The gate  $G_6$  is connected to the input of the gate inverter  $IV_{11}$ . A clock signal CLK is entered into the gates  $G_3$ ,  $G_4$ ,  $G_5$ ,  $G_6$ . When the clock signal CLK is in a high level, the gates  $G_3$  and  $G_6$  are opened, whereas when the clock signal CLK is in a low level, the gates  $G_4$  and  $G_5$  are opened.

When the transfer signal YSWb-1 is in a high level and also the output from the address decoder AD is in a high level, the NAND circuit  $NAND_1$  outputs a low level at the node S in response to the rising edge of the clock signal CLK. Next, the low level at the node S passes through the gate  $G_5$  upon receipt of the falling edge of the clock CLK. As a result, the switch selecting signal YSW is set to a low level, and the transfer signal YSWb is set to a high level. When the address decoder AD becomes a low level, or the level of the transfer signal YSWb-1 becomes a low level, the NAND circuit  $NAND_1$  outputs a high level at the node "S" upon receipt of the rising edge of the clock CLK irrelevant to the other output levels. Next, in response to the falling edge of the clock signal CLK, the gate  $G_5$  causes the high level of the node S to pass there through, so that the switch selecting signal YSW is set to a high level and the transfer signal YSWb is set to a low level. When the high level of the reset signal RST is inputted, the NOR circuit  $NOR_1$  necessarily outputs a low level, so that the transfer signal YSWb is set to a high level.

Next, operations of the DRAM memory shown in Fig. 4 explain as follow. At first, since the reset signal RST is inputted to all of the switch selecting circuits 1, the respective switch selecting signals YSW are set to low levels and the transfer signal YSWb is set to a high level.

Next, for example, when the switch selecting circuit 3-0 is selected by the address information, the output of the address decoder AD of the circuit 3-0 becomes a low level. Thus, the switch selecting circuit 3-0 outputs the switch selecting signal YSW-0 with the high level and the transfer signal YSWb-0 with the low level. Accordingly, in response to the switch selecting signal YSW-0 at the high level, the switch circuit 2-0 becomes activate and the data latch circuit 1-0 is connected to the data read/write amplifier 6 electrically to thereby perform the data transfer operation. Then, the transfer signal YSWb-0 at the low level is inputted to the switch selecting circuit 3-1 at the post stage, so that the switch

selecting circuit 3-1 outputs the switch selecting signal YSW-1 with the high level and the transfer signal YSWb-1 with the low level after 1 clock. At this time, since the transfer signal YSW-3 with the high level is entered into the switch selecting circuit 3-0 and the output of the address decoder AD of the circuit 3-0 turn low level, the switch selecting signal YSW-0 is set to a low level and the transfer signal YSWb-0 is set to a high level in response to the above-described 1 clock. As a result, the switch circuit 2-0 disconnected the data latch circuit 1-0 with the data read/write amplifier 6 and the switch circuit 2-1 becomes active. As described above, the transfer signal YSW having the high level is successively outputted from the selected switch selecting circuit to the post-staged switch selecting circuits every 1 clock, so that the data latch circuit 1 is successively connected with the data read/write amplifier 6. With the above-described operation, the information of the memory cell latched in the data latch circuits 1-0, 1-1, 1-2, and 1-3 is read from the memory cell at the selected address in the serial manner.

Referring now to Fig. 8, when the operation is in the data read mode, the data read signal DART becomes a high level. As previously explained in connection with Fig. 3, the data of the selected memory cell is read to each of the main-bit line pairs MBL0-3, MBLb0-3. Thereafter, the signal WS becomes a high level and the data of main-bit line pair is amplified the data latch signal DATG is produced in an one shot signal, and then the respective read data are fetched into the data latch circuit 1-0 ~ 1-3, and thereafter transferred to the data read line DBL0-3. On the other hand, the switch selecting circuit 3-0 is activated by the signal YSW-0 and enforce the switch circuit 2-0 active. As a result, the read data latched in the latch circuit 1-0 is sequentially started to be read. While this data is read, the respective main-bit line pairs MBL0-3, MBLb0-3 are initialized, and then the signal TG<sub>1</sub> becomes an active level, so that the data appearing on the next sub-bit line SBL1 is sensed and the read data is rewritten.

When the reading operation of the data latched in the latch circuit 1 is ended, the data latch signal DATG is again produced, and the data derived from the memory cell corresponding to the signal TG<sub>1</sub> is latched into the latch circuit 1, so that the data reading operation is continued. As a consequence, as shown in Fig. 8, the initializing period of the main bit line pairs can be masked, so that the data reading operation can be continued without any interrupt.

Referring now to Fig. 9, the data write signal DAWT becomes an active high level, the write data are inputted in input/output pin 8 in the serial manner prior to the selection of the word line, and thus these write data are sequentially latched into the latch circuit 1. During this operation, the word line is selected, the data of the memory cell selected by the word line is sensed and rewritten, and the data latch signal DATG is produced at a time when the write data are collected in the latch circuit 1. As a result, the write data are transferred to the

respective main-bit line pair and then are written into the memory cells. Although the initializing operation is thereafter carried out for the main-bit line pair, since the latch circuit 1 is disconnected, the subsequent write data can be sequentially latched into the latch circuit 1.

Fig. 10 is a circuit diagram of a data latch signal DATG generating circuit according to the first embodiment. Fig. 11 represents a timing chart for the data latch signal DATG generating circuit. A counter CA frequency-divides the clock signal CLK to generate timing signals C<sub>1</sub> to C<sub>4</sub>. The timing signals C<sub>1</sub> and C<sub>2</sub> are supplied to a NAND circuit D<sub>2</sub>, and an output from this NAND circuit D<sub>2</sub> is controlled in response to a write enable signal WM having an active high level. On the other hand, the timing signals C<sub>3</sub> and C<sub>4</sub> are supplied to a NAND circuit D<sub>3</sub>, and an output from this NAND circuit D<sub>3</sub> is controlled in response to a read enable signal RM having an active high level. As a consequence, the data latch signal DATG is generated by another NAND circuit NAND<sub>4</sub> for inputting the outputs derived from the NAND circuits NAND<sub>2</sub> and NAND<sub>3</sub>, and this data latch signal DATG owns different timings during the data reading operation and the data writing operation. This implies that all of the data are not written into this memory during the data writing operation, but since a portion of data is rewritten by using the original data, after the read data is defined, namely the refresh operation can be sufficiently performed, the data latch signal DATG during the data writing operation is raised.

Fig. 12 is a circuit diagram for showing a data latch signal DATG generating circuit, according to a second embodiment of the present invention, used in the memory. The counter CA inputs the clock signal CLK to thereby produces timing signals C<sub>1</sub> and C<sub>4</sub>. Upon receipt of inverted signals of these timing signals C<sub>1</sub> and C<sub>4</sub>, a data latch signal DATG is generated by a NAND circuit NAND<sub>5</sub> (see Fig. 11).

A data read cycle and a data write cycle of the memory to which the data latch signal DATG generating circuit of Fig. 12 has been applied will now be explained with reference to Fig. 13 and Fig. 14 respectively.

In the data read cycle, the information of the memory cell selected by raising the switch selecting signal YSW during a front half period of the rising condition of the data latch signal DATG is transferred to the data read/write amplifier 6 under such a condition that the levels of the main bit line pair MSL and MSLb can be sufficiently defined. In the data write cycle, the writing operation is performed immediately after the write signal DAWT is raised. Since the data latch signal DATG is raised for a long time period, the level corresponding to the data to be written can be written in to the main bit line pairs MBL and MBLb during a sufficiently long time period. As a result, there is such an advantage that the writing level to the memory cell can be improved. Also, there is another advantage that since the data latch signal DATG is activated during the same time period even in the write cycle and the read cycle, the circuit arrangement of this data latch signal generating circuit can be

simplified. However, in the actual case, since the cycles are not divided during the data reading operation and the data writing operation similar to that of the first embodiment, the cycles must be sufficiently prolonged in order that the data writing operation is carried out after the read data has been sufficiently defined.

It should be noted that the present invention is not limited to the above-described embodiment, but may be modified. For instance, a total number of the sub-bit lines and/or the word lines may be properly changed. Also, only four sets of the main/sub-bit line arrangements are employed in this embodiment. Alternatively, at least two sets of the main/sub-bit line arrangements are sufficient. Furthermore, the above-described embodiment has described that the levels at the respective wire lines were defined at the high levels or the low levels. Alternatively, these levels may be properly changed. Accordingly, the characteristics and the conducting types of these pMOS transistors/nMOS transistors are varied in accordance with the above level changes.

As previously described in detail, since the sensing operations of the main bit lines can be performed while the data is read and written, the data can be read/written without any interrupt. As a consequence, the present invention can provide such an advantage that the data transfer efficiency can be increased.

## Claims

### 1. A semiconductor memory device comprising:

a plurality of sub-bit lines;  
a sense amplifier provided in common to said plurality of sub-bit lines and receiving a data signal from a first one of said plurality of sub-bit lines;  
a main-bit line operatively coupled to said sense amplifier to receive an output of said sense amplifier;  
a data latch circuit provided to latch data appearing on said main-bit line; and  
means for transferring a data signal of a second one of said plurality of sub-bit lines to said sense amplifier during said data latch circuit being accessed to read out data latched in said data latch circuit.

2. The semiconductor memory device claimed as claim 1, wherein said sense amplifier responds to the data signal of said second one of said plurality of bit lines and drives said main-bit line during said data latch circuit being accessed.

3. The semiconductor memory device claimed as claim 1, further comprising an additional sense amplifier coupled to drive said main-bit line in response to the output of said sense amplifier, said data latch circuit being activated to latch the data on

said main-bit line after said additional sense amplifier drives said main-bit line.

### 4. A semiconductor memory device comprising:

a plurality of sub-bit lines;  
a sense amplifier provided in common to said plurality of sub-bit lines;  
a main-bit line coupled to said sense amplifier;  
a data latch circuit temporarily latching first data to be written,  
first means for transferring said first data from said data latch circuit to said main bit line to thereby allow said sense amplifier to drive a first one of said sub-bit lines in response to said first data; and  
second means for disconnecting said data latch circuit from said main-bit line during said data latch circuit being controlled to latch second data to be written, to thereby allow said sense amplifier prepare driving a second one of said sub-bit lines in response to said second data.

### 5. A semiconductor memory device comprising:

a plurality of sub-bit lines, said sub-bit lines being divided into a plurality of groups each having a plurality of sub-bit lines;  
a plurality of word lines intersecting each of said sub-bit lines;  
a plurality of memory cells disposed at intersections of said sub-bit lines and said word lines;  
a plurality of sense amplifiers each provided in common to an associated one of said groups to receive a data signal from a first one of said sub-bit lines belonging to said associated one of said groups;  
a plurality of main-bit lines each operatively coupled to an associated one of said sense amplifiers;  
a plurality of data latch circuits each provided for an associated one of said main-bit lines to latch data appearing on said associated one of main-bit lines; and  
means for transferring a data signal of a second one of said sub-bit lines belonging to each of said groups to a corresponding one of said sense amplifiers during each of data latch circuits being accessed to read out data latched therein.

6. The semiconductor memory device as claimed in claim 5, wherein said data latch circuits are accessed in sequence to read the data latched in said data latch circuits in series.

### 7. A semiconductor memory device comprising:

a plurality of first sub-bit lines;  
 a plurality of second sub-bit lines;  
 first and second sense amplifiers provided  
 respectively to said plurality of first and second  
 sub-bit lines; 5  
 first and second main-bit lines provided respec-  
 tively to said first and second sense amplifiers;  
 first and second data latch circuits provided  
 respectively to said first and second main-bit  
 lines; 10  
 a data read bus provided to said first and sec-  
 ond data latch circuits;  
 a data write bus provided to said first and sec-  
 ond data latch circuits;  
 read means for said first amplifier receiving a 15  
 first read-data from a first one of said plurality  
 of first sub-bit lines, said second amplifiers  
 receiving a second read-data from said first  
 one of said plurality of second sub-bit lines,  
 said first data latch circuit latching said first 20  
 read-data appearing on said first main-bit lines,  
 said second data latch circuit latching said sec-  
 ond read-data appearing on said second main-  
 bit lines, and switching from said first one of  
 said plurality of first sub-bit lines to a second 25  
 one thereof and from said first one of said plu-  
 rality of second sub-bit lines to a second one  
 thereof to access said second one of said plu-  
 rality of first and second sub-bit lines during  
 said first and second data latch circuits being 30  
 accessed to read out said first and second  
 read-data latched in said first and second data  
 latch circuits into said data read bus;  
 write means for transferring a first write-data  
 latched in said first data latch circuit via said 35  
 first main-bit line to said first one of said plu-  
 rality of first sub-bit lines and a second write-data  
 latched in said second data latch circuit via said  
 second main-bit line to said first one of said plu-  
 rality of second sub-bit lines, and switching 40  
 from said first one of said plurality of first sub-  
 bit lines to said second one thereof and from  
 said first one of said plurality of second sub-bit  
 lines to said second one thereof to access said  
 second one of said plurality of first and second 45  
 sub-bit lines during said first and second data  
 latch circuits being accessed to latch a third  
 write-data and a fourth write-data respectively  
 to be written into said second one of said plu-  
 rality of first and second sub-bit lines. 50

data appearing on said data write line by said write  
 signal being active and transferring the latched data  
 of said second flip-flop to said main-bit line when  
 said data latch signal becomes active during said  
 write signal being active.

8. The semiconductor memory device claimed as  
 claim 8, wherein said data latch circuit inputs a data  
 latch signal, a read signal and a write signal,  
 said data latch circuit has a first flip-flop 55  
 formed by said read signal being active and latching  
 said read data in said first flip-flop when said data  
 latch signal becomes active during said read signal  
 being active, a second flip-flop latching said write

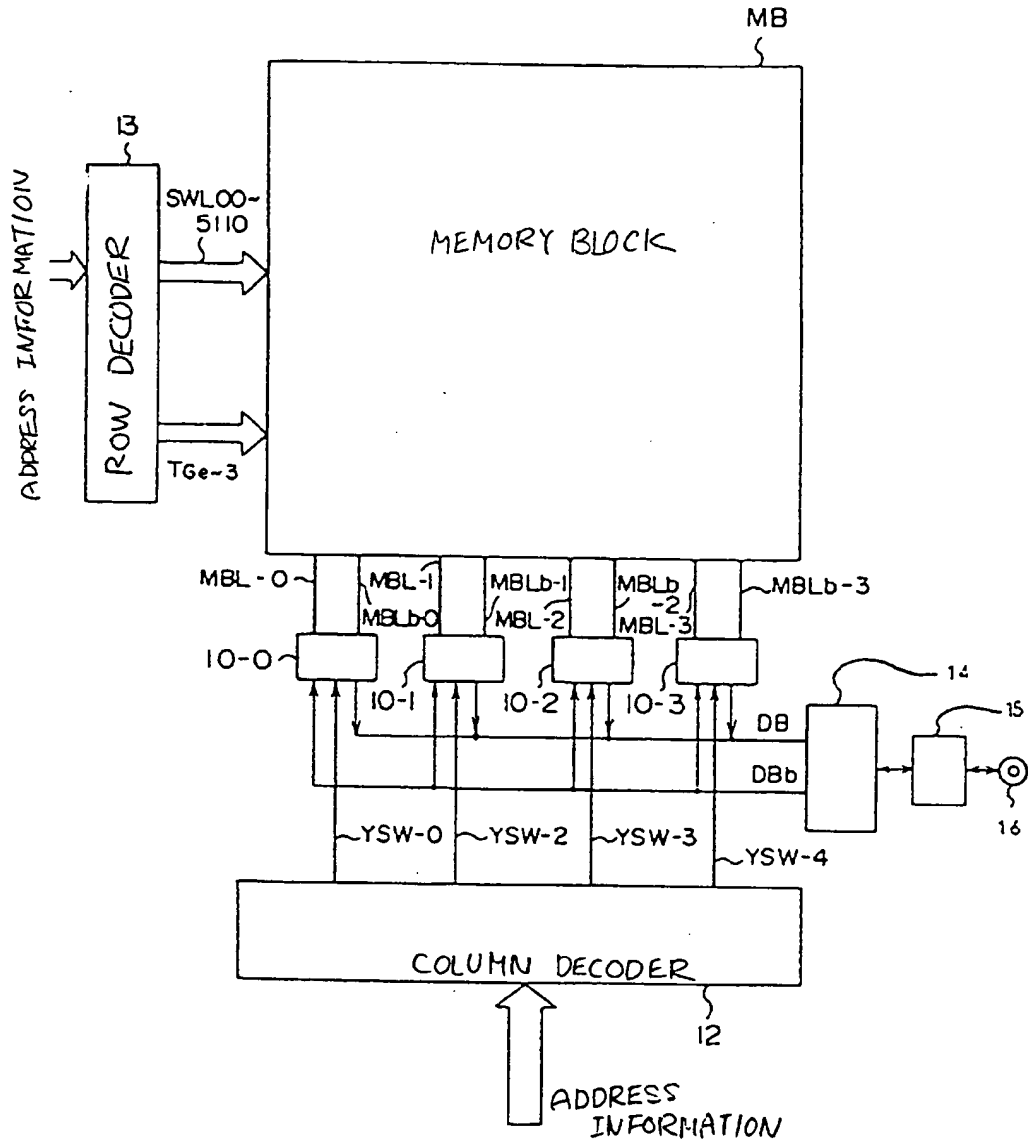


Fig. 1 [prior art]

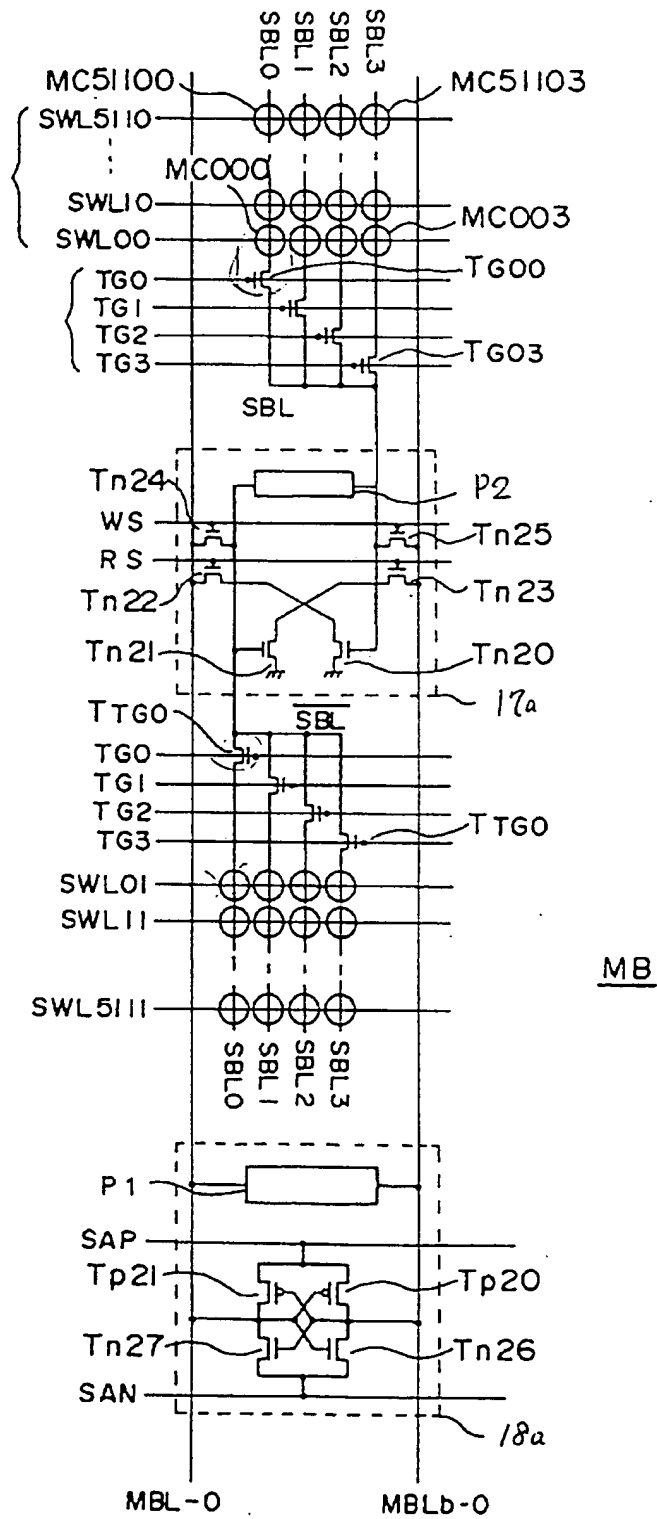


Fig. 2

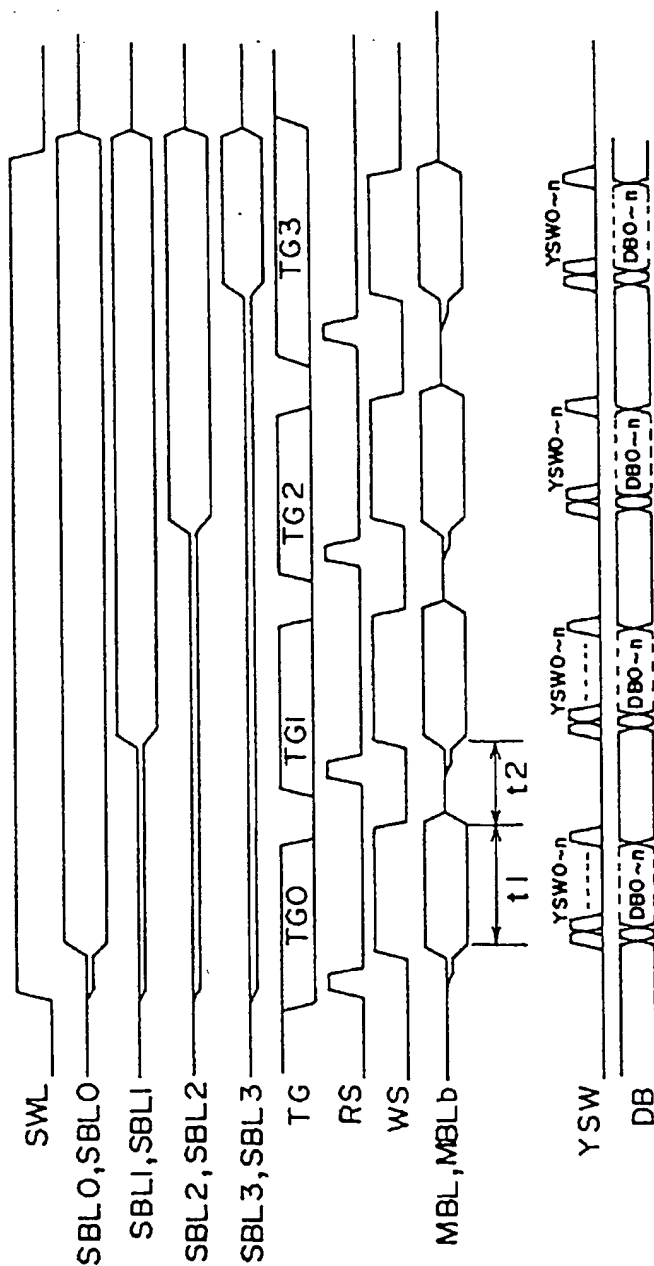


Fig. 3 [prior art]

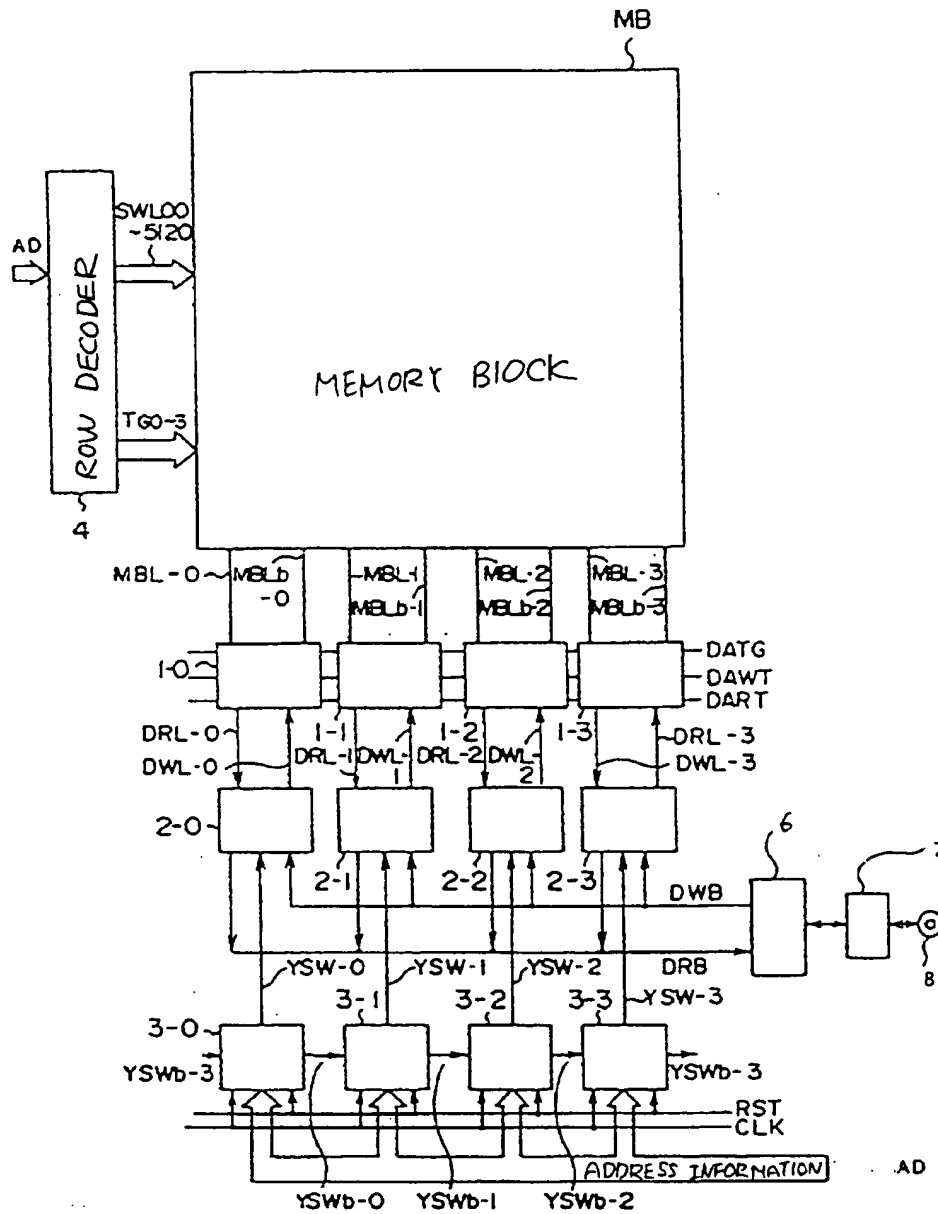


Fig. 4

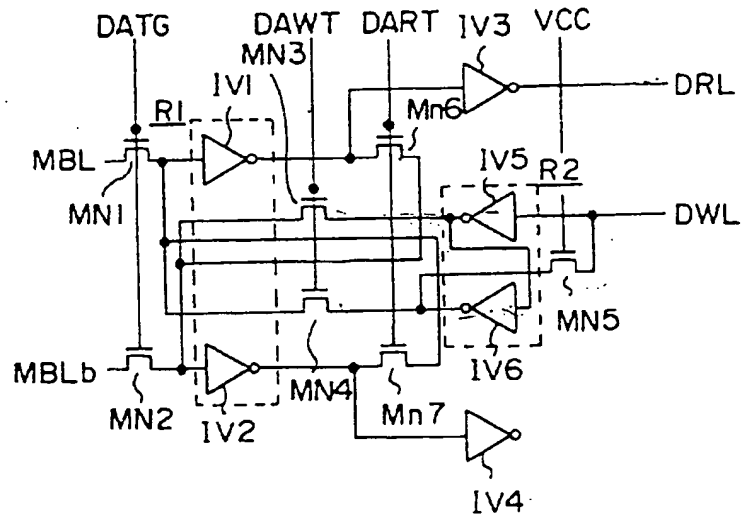


Fig. 5

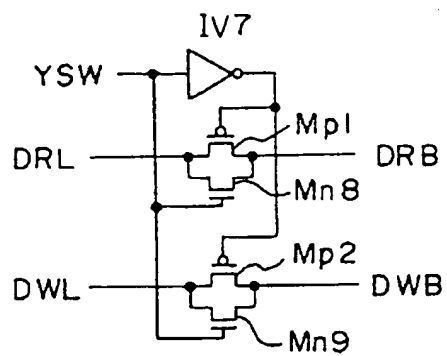


Fig. 6

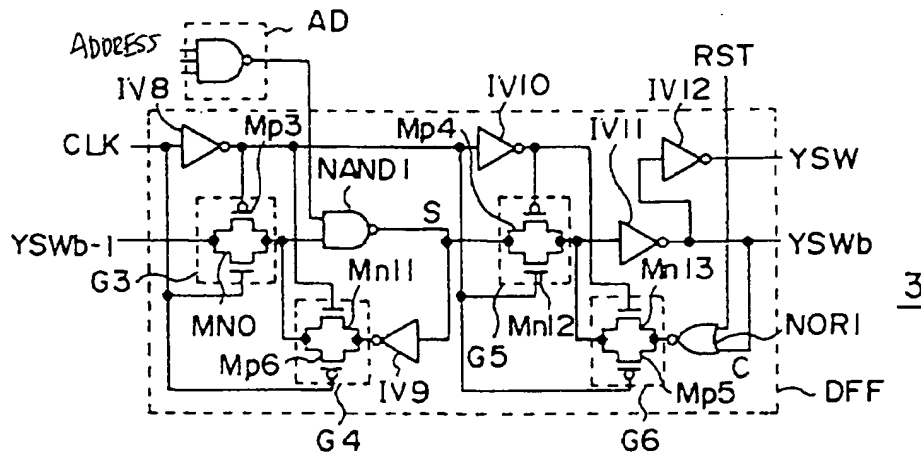


Fig. 7

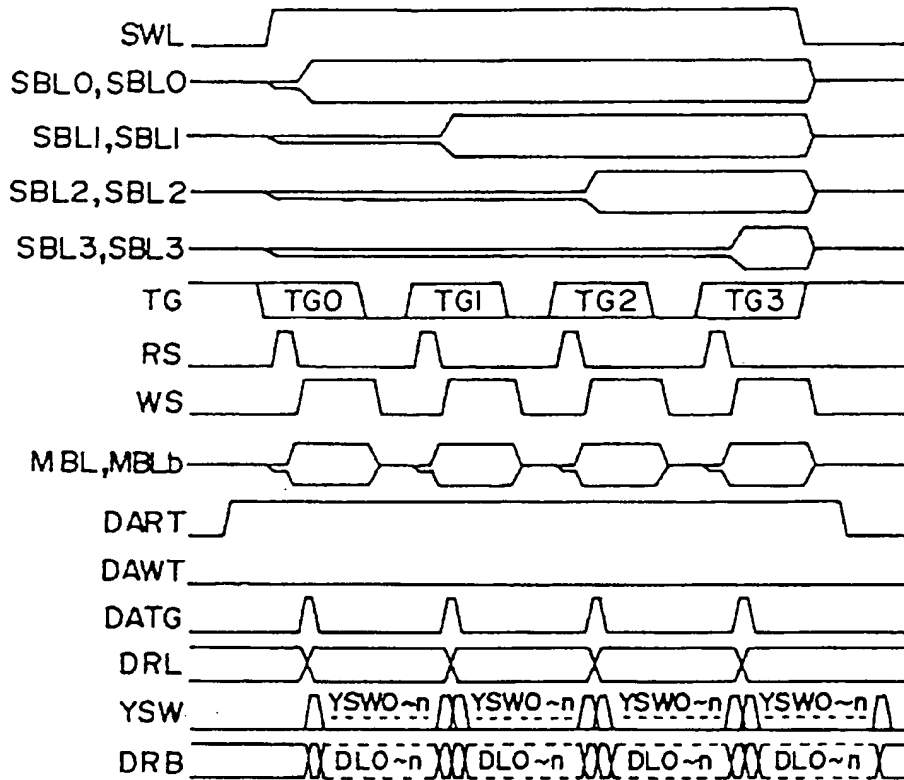


Fig. 8

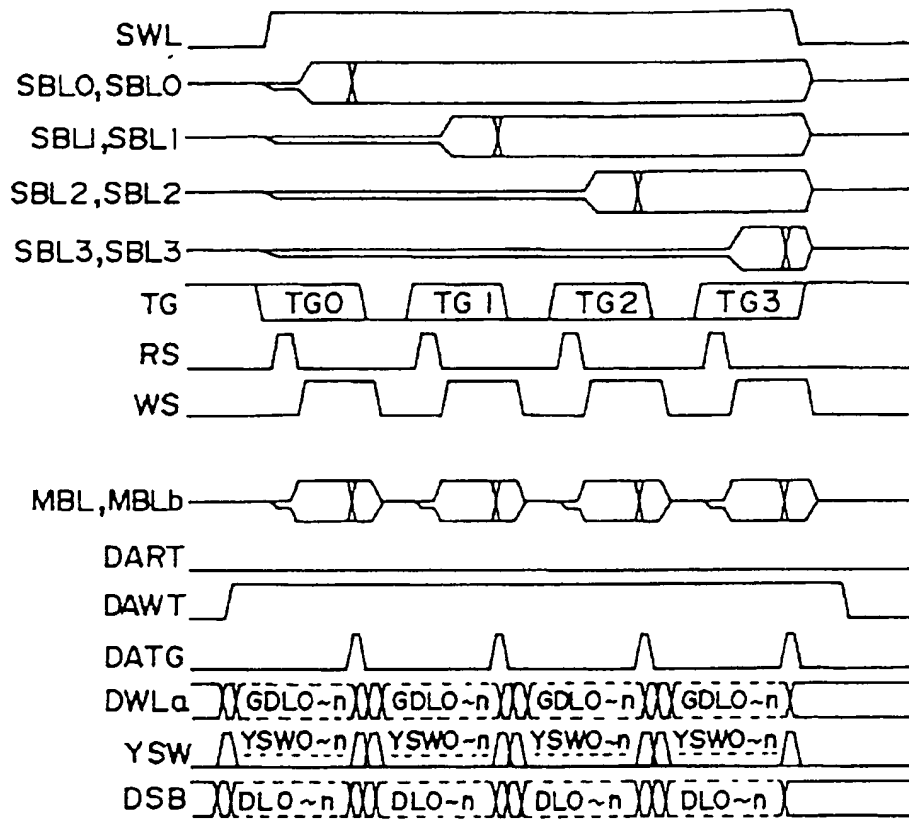


Fig. 9

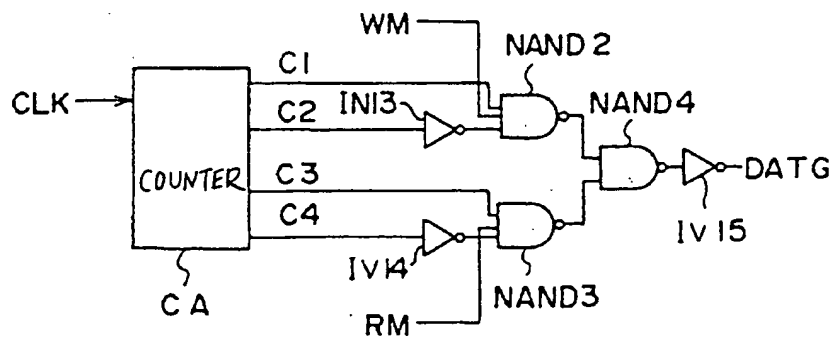


Fig. 10

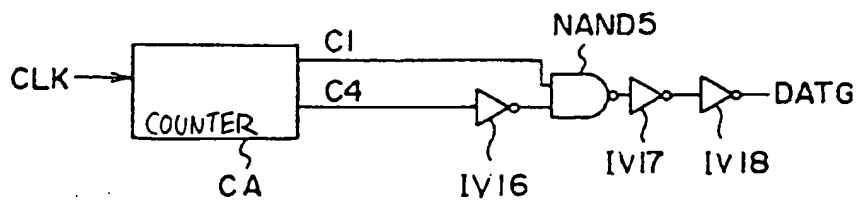
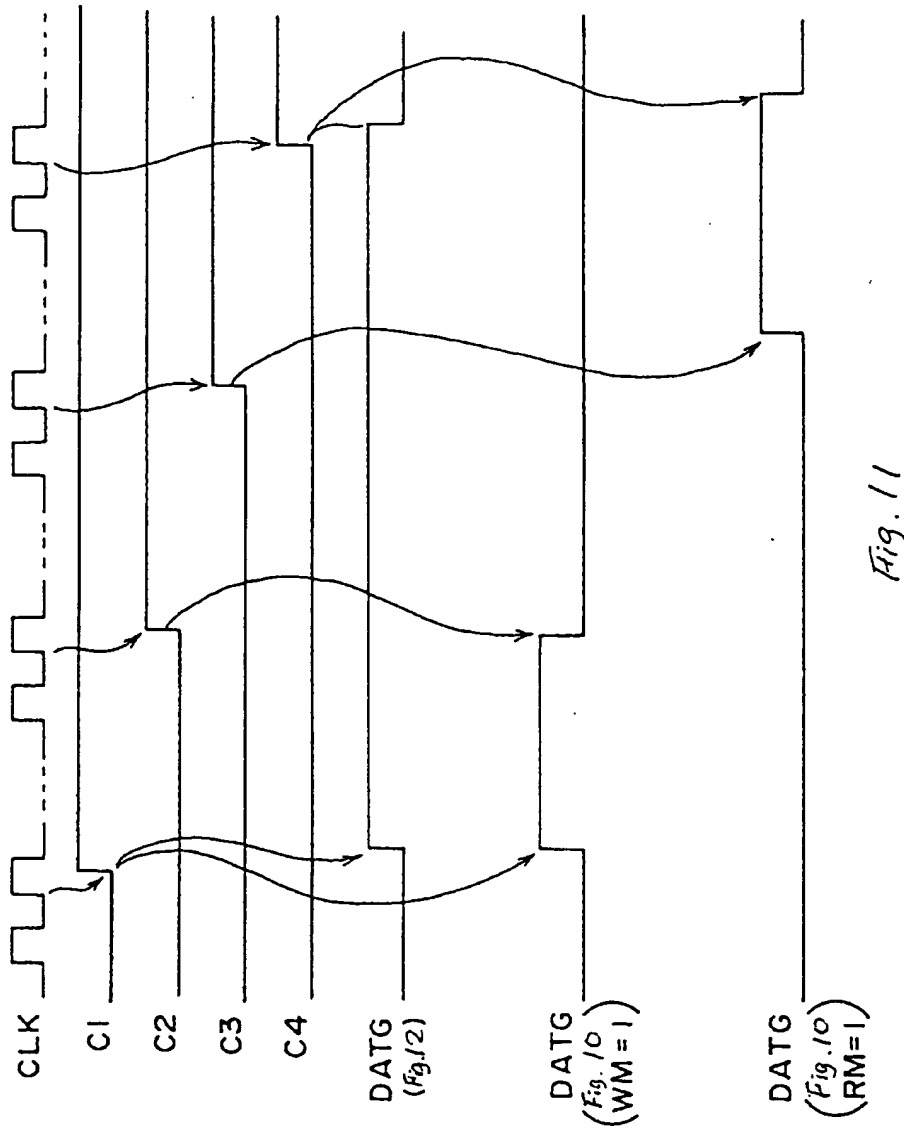


Fig. 12

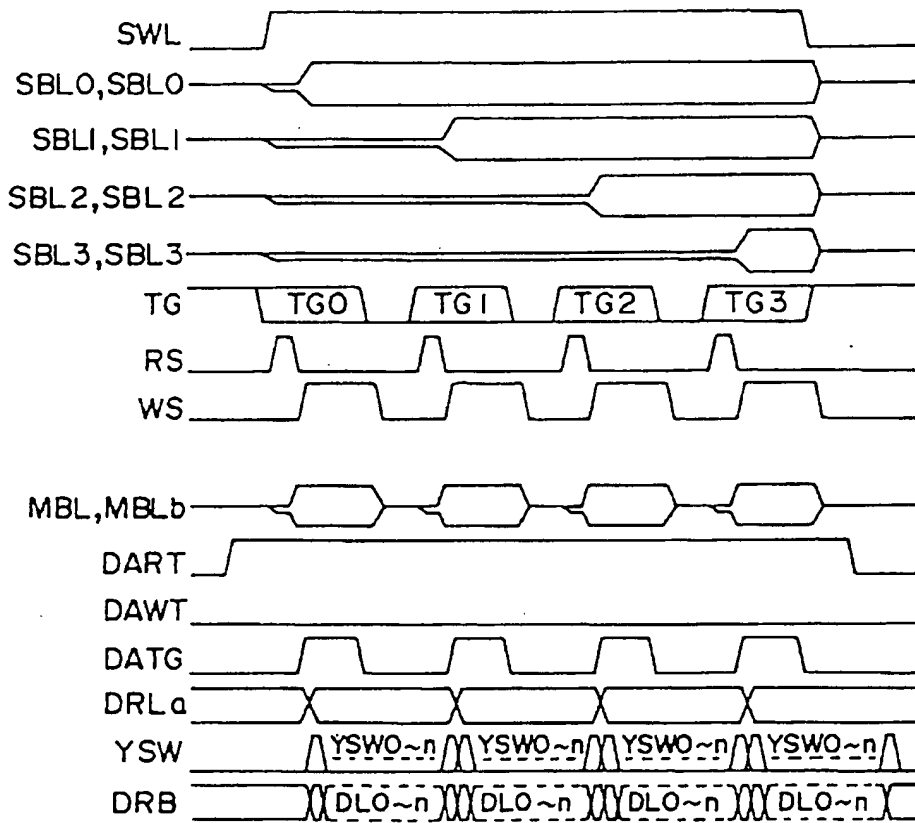


Fig. 13

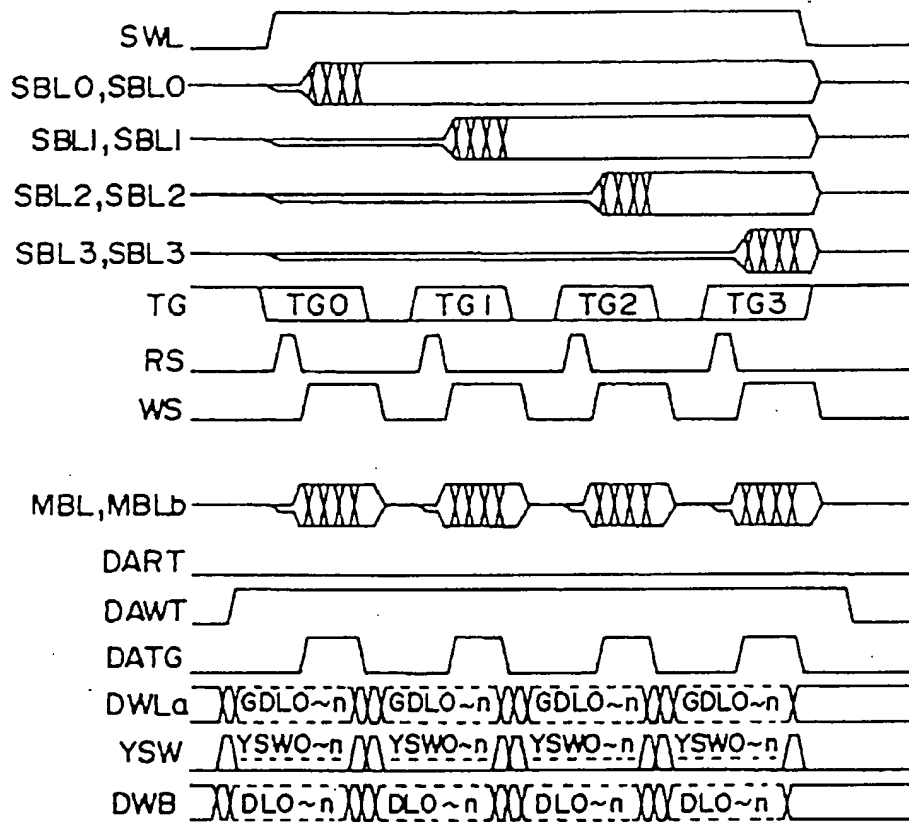


Fig. 14